WHAT IS CLAIMED IS:

1. A method of forming a source/drain of a transistor, comprising:

forming a recess in a substrate adjacent a gate of said transistor;

forming a deep doped region below a bottom surface of said recess; and

epitaxially growing a semiconductor material within said recess to form said source/drain.

2. The method as recited in Claim 1 further comprising forming a lightly doped drain region adjacent said gate.

3. The method as recited in Claim 1 wherein said semiconductor material is silicon.

4. The method as recited in Claim 1 wherein said forming said deep doped region is performed by an ion implantation process.

5. The method as recited in Claim 4 wherein said ion implantation process comprises implanting one of P-type ions and N-type ions.

6. A transistor, comprising:

a gate formed on a substrate; and

a source/drain formed in a recess of said substrate adjacent said gate and including:

a lightly doped drain region adjacent said gate, and

a deep doped region below a bottom surface of said recess.

7. The transistor as recited in Claim 6 further comprising another source/drain formed in another recess of said substrate adjacent said gate and including:

a lightly doped drain region adjacent said gate; and

a deep doped region below a bottom surface of said another recess.

8. The transistor as recited in Claim 6 wherein said source/drain comprises an epitaxially grown semiconductor material.

9. The transistor as recited in Claim 6 further comprising spacers on opposing walls of said gate.

10. The transistor as recited in Claim 6 wherein said gate and source/drain comprise a contact.

11. A method of forming a transistor, comprising:

providing a gate on a substrate, including:

forming a gate dielectric over said substrate, and

forming a gate electrode over said gate dielectric; and

providing a source/drain, including:

forming a recess in said substrate adjacent said gate,

forming a deep doped region below a bottom surface of said recess; and

epitaxially growing a semiconductor material within said recess to form said source/drain.

12. The method as recited in Claim 11 wherein said providing said source/drain further includes forming a lightly doped drain region adjacent said gate.

13. The method as recited in Claim 11 wherein said semiconductor material is silicon.

14. The method as recited in Claim 11 wherein said forming said deep doped region is performed by an ion implantation process.

15. The method as recited in Claim 14 wherein said ion implantation process comprises implanting one of P-type ions and N-type ions.

16. The transistor as recited in Claim 11 further comprising providing another source/drain, including:

forming another recess in said substrate adjacent said gate;

forming a deep doped region below a bottom surface of said another recess; and

epitaxially growing a semiconductor material within said another recess to form said another source/drain.

17. The method as recited in Claim 16 wherein said providing said another source/drain further includes forming a lightly doped drain region adjacent said gate.

18. The method as recited in Claim 16 wherein said semiconductor material is silicon.

19. The method as recited in Claim 11 wherein said providing said gate further includes forming spacers on opposing walls of said gate dielectric and gate electrodes.

20. The method as recited in Claim 11 wherein said providing said gate and said source/drain further include performing a salicide process to form contacts thereon.